

CLAIMS

We claim:

1 1. A method comprising:
2 dividing a physical address space into a plurality of
3 segments;
4 computing an interim first address from a physical
5 address from the physical address space;
6 computing an interim base value from a base value
7 associated with the physical address;
8 comparing the interim first address and the interim
9 base value to determine whether the physical address can be
10 validly translated to obtain a translated address; and
11 if the physical address can be validly translated,
12 combining the physical address with an offset value to
13 obtain the translated address.

1 2. The method of Claim 1, further comprising:
2 determining a memory type of the translated address.

1 3. The method of Claim 2, wherein determining
2 comprises:
3 reading the memory type from the base value associated
4 with the physical address.

1 4. The method of Claim 1, wherein computing the
2 interim first address comprises:
3 determining which bits of the physical address should
4 be retained in the interim first address for comparison with
5 the interim base value,
6 and wherein computing the interim base value comprises:

7 determining which bits of a base value should be
8 retained in the interim base value for comparison with the
9 interim first address.

1 5. The method of Claim 4, wherein determining which
2 bits of the physical address and which bits of the base
3 value should be retained for comparison comprises:

4 applying a mask value to each of the physical address
5 and the base value, the mask value associated with the
6 physical address.

1 6. The method of Claim 1, wherein combining
2 comprises:

3 determining which bits of the physical address should
4 be retained in the translated address; and

5 substituting bits from the offset value for bits of the
6 physical address which are not to be retained in the
7 translated address.

1 7. The method of Claim 6, wherein determining which
2 bits comprises:

3 applying a mask value to the physical address, the mask
4 value associated with the physical address.

1 8. The method of Claim 1, further comprising:
2 issuing a fault alert.

1 9. The method of Claim 8, wherein issuing the fault
2 alert comprises:

3 issuing a notice that no mapping exists for the
4 physical address.

1 10. The method of Claim 8, wherein issuing the fault
2 alert comprises:

3 issuing a notice that an attempt has been made to
4 access a particular segment.

1 11. The method of Claim 10, wherein issuing the notice
2 comprises:

3 detecting whether a fault bit has been set for the
4 particular segment.

1 12. The method of Claim 1, wherein if the physical
2 address cannot be validly translated, the translated address
3 is the same as the physical address.

1 13. An apparatus comprising:

2 a memory having a first address space divided into a
3 plurality of segments;

4 comparison logic circuitry coupled to the memory to
5 create an interim first address from a first address from
6 one of the plurality of segments, to create an interim base
7 value, and to compare the interim first address and the
8 interim base value to determine whether the first address
9 belongs to a segment that can be validly translated to
10 obtain a second address; and

11 combination logic circuitry coupled to the comparison
12 logic circuitry and to the memory, the combination logic
13 circuitry to combine the first address with an offset value
14 to obtain the second address if the comparison logic
15 circuitry indicates that the first address can be validly
16 translated.

1 14. The apparatus of Claim 13, wherein the comparison
2 logic circuitry comprises:

3 masking circuitry to apply a mask value to the first
4 address to obtain the interim first address and to apply the

5 mask value to a base value to obtain the interim base value,
6 the mask value associated with the first address.

1 15. The apparatus of Claim 13, wherein the combination
2 logic circuitry comprises:

3 masking circuitry to apply a mask value to the first
4 address to determine which bits of the first address should
5 be retained in the second address; and

6 substitution circuitry to substitute bits from the
7 offset value for bits of the first address which are not to
8 be retained in the second address.

1 16. The apparatus of Claim 13, further comprising:
2 fault detection circuitry coupled to the comparison
3 logic circuitry, the fault detection circuitry to detect and
4 issue fault alerts.

1 17. A system comprising:
2 a processor;
3 memory coupled to the processor, the memory having a
4 first address space divided into a plurality of segments;
5 comparison logic circuitry coupled to the memory to
6 create an interim first address from a first address from
7 one of the plurality of segments, to create an interim base
8 value, and to compare the interim first address and the
9 interim base value to determine whether the first address
10 belongs to a segment that can be validly translated to
11 obtain a second address; and

12 combination logic circuitry coupled to the comparison
13 logic circuitry and to the memory, the combination logic
14 circuitry to combine the first address with an offset value
15 to obtain the second address if the comparison logic
16 circuitry indicates that the first address can be validly
17 translated.

18 18. The system of Claim 17, wherein the comparison
19 logic circuitry comprises:

20 masking circuitry to apply a mask value to the first
21 address to obtain the interim first address and to apply the
22 mask value to a base value to obtain the interim base value,
23 the mask value associated with the first address.

1 19. The system of Claim 17, wherein the combination
2 logic circuitry comprises:

3 masking circuitry to apply a mask value to the first
4 address to determine which bits of the first address should
5 be retained in the second address; and

6 substitution circuitry to substitute bits from the
7 offset value for bits of the first address which are not to
8 be retained in the second address.

1 20. The system of Claim 17, further comprising:

2 fault detection circuitry coupled to the comparison
3 logic circuitry, the fault detection circuitry to detect and
4 issue fault alerts.